UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,389	11/10/2003	Melvin Bringas Alviar	TI-36227 (032350.B528)	6375

23494 7590 02/08/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
SCHATZ, CHRISTOPHER	

ART UNIT	PAPER NUMBER
1733	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,389	ALVIAR, MELVIN BRINGAS	
	Examiner	Art Unit	
	Christopher T. Schatz	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *13-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-12 in the reply filed on November 30, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Claims 13-22 are withdrawn from consider as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 6, 8, 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 2003/0094241 A1) in view of Higashi et al. (US 2001/0001469 A1).

Huang et al. discloses a method for adhering an integrated circuit 251 (paragraph 0004, 0023) to a substrate comprising: receiving a boat 13 configured to hold a plurality of substrates at a first position 111 (figure 3, paragraph 0019, 0022), the substrates having a first surface configured to support an integrated circuit 151 (figure 3); heating the boat of substrates at the

first position 111; transferring the boat of substrates from the first position to a second position 113 (paragraph 0023); positioning the integrated circuit on the first surface of a selected one of the plurality of substrates at the second position (paragraph 0023, figures 2 and 4). Applicant should note that although Huang et al. refers to 17 as a substrate, examiner asserts that 17 as defined by the reference reads on applicants term matrices (20) and that 17 consists actually consists of *three* substrates since there are three locations on 17 that can support an integrated circuit. The reference is silent as to a method wherein the integrated circuit comprises an adhesive surface operable to adhere the integrated circuit to the selected substrate.

Higashi et al. discloses a method for adhering an integrated circuit 3 to a substrate 4 wherein the integrated circuit comprises an adhesive surface operable to adhere the integrated circuit to the selected substrate. Furthermore, the reference discloses that an adhesive surface capable of adhering the integrated circuit to the substrate can be present on the integrated circuit as an alternative to having the adhesive on the substrate (paragraph 0036, 0042). Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to position an integrated circuit on one of the plurality of substrates wherein the integrated circuit has an adhesive surface capable of adhering the integrated circuit to the substrate as an alternative to the surface of the substrate having an adhesive surface as taught by Higashi et al. above in the method of adhering an integrated circuit to a substrate as taught by Huang et al. above.

As to claim 2, Higashi et al. discloses a method wherein the adhesive surface is selected so as to melt at a predetermined temperature (paragraph 0039-0040). As to claim 6, Huang et al. discloses a method wherein heating the boat of substrates at the first position comprises

positioning a portion of the substrates in the boat proximate a heating element such that warping of the substrates is prevented (paragraph 0022). As to claim 8, Huang et al. discloses that use of a vacuum chuck is employed to properly hold and position the substrates on the boat. While the reference does not explicitly disclose that vacuum chucking occurs at the second position, one of ordinary skill in the art would have readily appreciated chucking would be necessary because proper positioning of the substrate is critical during the bonding process. As to claim 10, Huang et al. discloses a method further comprising receiving the boat of substrates at a feeding system, the feeding system operable to transport the boat to the first position (figures 2 and 4). As to claim 11, examiner asserts that one of ordinary skill in the art would have readily recognized that bond line and bond line thickness uniformity is critical to the quality of the final product, and thus taking measurements of said thickness would allow one to determine the quality of the bond formed.

4. Claims 1, 2, and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. as applied above, and in further view of Dell.

Huang et al. discloses a method as stated above, but the reference is silent as to a method wherein the integrated circuit comprises an adhesive surface operable to adhere the integrated circuit to the selected substrate. Dell discloses a method for adhering an integrated circuit to a substrate, wherein the integrated circuit comprises an adhesive surface operable to adhere the integrated circuit to the selected adhesive (see section II). The reference further discloses that an adhesive surface capable of adhering the integrated circuit to the substrate is advantageous because having said adhesive surface allows 100% adhesive coverage and prevents die cracking when subjecting the bonded die to long cycles of extreme temperature cycling conditions

(section III). Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to position an integrated circuit on one of the plurality of substrates wherein the integrated circuit has an adhesive surface capable of adhering the integrated circuit to the substrate as taught by Dell above in the method of adhering an integrated circuit to a substrate as taught by Huang et al. above.

As to claim 2, examiner asserts that since the Dell reference discusses the use of the same adhesive as applicant discusses in the specification (NEX 130C), one of ordinary skill in the art would have readily recognized that said adhesive melts at a predetermined temperature. As to claim 6, 8, 10, and 11, Huang et al. meets the limitations of said claims for the reasons presented above. As to claims 7 and 9, examiner asserts that because the Dell reference uses the same adhesive as applicant, one of ordinary skill in the art would have readily recognized to heat the substrates to applicant's claimed temperature such that the adhesive can properly melt.

5. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. and Dell as applied above, and in further view of Kawasaki et al. (US 2003/0038379).

Huang et al. and Dell disclose a method as stated above, but the references are silent as to the specific structure of the substrate. Kawasaki et al. discloses a method for adhering an IC chip to a substrate, wherein said substrate comprises: a first layer 14 of film comprising an outer film surface; a second layer comprising a conductive material 11, 21, the second layer positioned adjacent to the outer film surface of the first layer (figure 4f, paragraph 0028); and a third layer 24 comprising a solder mask positioned adjacent to the second layer, the third layer selected so as to not melt at the predetermined temperature, an outer surface of the third layer configured to support the integrated circuit (figure 4f, figure 7, paragraphs 0045, 0061). The use of a substrate

with the above described structure is advantageous because, as disclosed by Kawasaki et al., said substrate allows for reliable bonding of IC's without warpage (paragraph 0017). Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method disclosed by Huang et al. and Dell such that the substrate of Kawasaki et al. is used in order to prevent warpage of the substrate during bonding as taught by Kawasaki et al. above.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. and Dell as applied above, and in further view of Dietz et al. '402.

Huang et al. and Dell disclose a method as stated above, but the references are silent as to a method of testing for voids in the bond between the substrate and a circuit. Dietz et al. discloses a method of bonding an integrated circuit to a substrate wherein after the bonding occurs an adherence test is performed to determine if voids are present (column 9, lines 52-62). Testing for voids is advantageous because, as disclosed by Dietz et al., the presence of voids significantly affects the strength of the bond between the circuit and the substrate (column 9, line 63- column 10, line 14). Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to perform an adherence test to determine if voids are present between the substrate and the circuit as taught by Dietz et al. above in the method of adhering an integrated circuit to a substrate as forth above by Huang et al. and Dell.

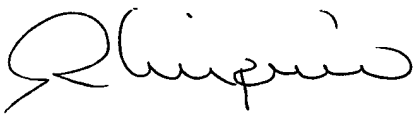
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Christopher T. Schatz** whose telephone number is **571-272-1456**. The examiner can normally be reached on 8:00-5:30, Monday -Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on 571-272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CTS



RICHARD CRISPINO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700